What is Claimed Is:



Integrated circuit between at least two circuit components, the method comprising:

providing, using the GPIO line, a first input from a first circuit component to the integrated circuit during a first time; providing, using the GPIO line, a first output from the integrated circuit to a

second circuit component during a second time; and wherein the first circuit component and the second circuit component are concurrently coupled to the GPIO line.

[c2]

2. The method of Claim 1, wherein the step of providing the first input includes providing the first input at a low frequency relative to a switching frequency of the GPIO line.

[c3]

3. The method of Claim 2, wherein the first time is at least in part concurrent with the second time.

[c4]

4. The method of Claim 1, wherein the first time is different from the second time.

[c5]

5. The method of Claim 1, further comprising the step of providing, using the GPIO line, a second input from the first circuit component to the integrated circuit during a third time different from the first time.

[c6]

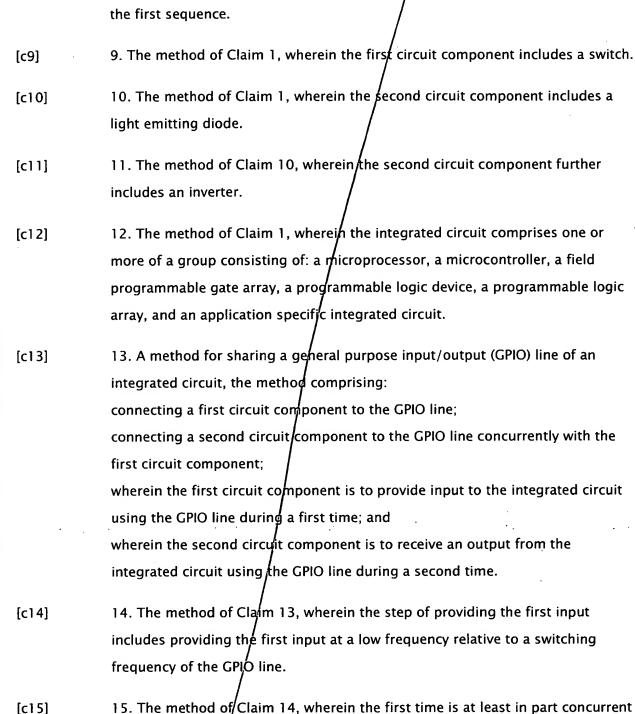
6. The method of Claim 1, further comprising the step of providing, using the GPIO line, a second output from the integrated circuit to the second circuit component during a third time different from the second time.

[c7]

7. The method of Claim 1, wherein the step of providing a first input comprises the step of configuring the GPIO line as an input line during a portion of the first time, and the step of providing a first output comprises the step of configuring the GPIO line as an output line during the second time.

[c8]

8. The method of Claim 7, wherein: the portion includes a first sequence of processing cycles; and



the second time includes a second sequence ϕ f processing cycles different from

[c17]

[c16]

17. The method of Claim 13, further comprising the steps of:

16. The method of Claim 13, wherein the first time is different from the second

with the second time.

time.

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[c22]

[c23]

configuring the GPIO line as an input line during a portion of the first time; and configuring the GPIO line as an output life during the second time period.

- 18. The method of Claim 17, wherein: [c18]the portion includes a first sequence of processing cycles; and the second time includes a second sequence of processing cycles different from the first sequence.
- 19. The method of Claim 13, wherein the first circuit component includes a [c19]switch.
- [c20] 20. The method of Claim 13, wherein the second circuit component includes a light emitting diode.
- 21. The method of Claim 20, wherein the second circuit component further [c21] includes an inverter.
 - 22. The method of Claim 13, wherein the integrated circuit is one of a group consisting of: a microprocessor, a microcontroller, a field programmable gate array, a programmable logic/device, a programmable logic array, and an application specific integrated circuit.
 - 23. An electrical circuit having circuit components in electrical communication with an integrated circuit, the circuit being adapted to share a general purpose input/output (GPIO) line of the integrated circuit among at least two circuit components external to the integrated circuit, the circuit comprising: a first circuit component connected to the GPIO line; a second circuit component connected to the GPIO line concurrently with the first circuit component; the integrated circuit being adapted to receive an input from the first circuit component via the GPIO line during a first time; and the integrated circuit being adapted to provide an/output to the second circuit component via the GPIO line during a second time!
- 24. The circuit of Claim 23, wherein the first circuit is adapted to provide the [c24]first input at a low frequency relative to a switching frequency of the GPIO line.
- [c25] 25. The circuit of Claim 24, wherein the first time is at least in part concurrent

[c26]

time.



26. The circuit of Claim 23, wherein the first time is different from the second

- [c27] 27. The circuit of Claim 23, wherein the GPIO line is configured as an input line during a portion of the first time, and the GPIO line is configured as an output line during the second time.
- [c28] 28. The circuit of Claim 27, wherein the portion includes a first sequence of processing cycles, and the second time includes a second sequence of processing cycles different from the first sequence.
- [c29] 29. The circuit of Claim 23, wherein the first circuit component includes a switch.
- [c30] 30. The circuit of Claim 23, wherein the second circuit component includes a light emitting diode.
- [c31] 31. The circuit of Claim 30, wherein the second circuit component further includes an inverter.
- [c32] 32. The circuit of Claim 23, wherein the integrated circuit comprises at least one of a group consisting of: a microprocessor, a microcontroller, a field programmable gate array, a programmable logic device, a programmable logic array, and an application specific integrated circuit.
- [c33] 33. In a system comprising electrical circuitry and components:

 an integrated circuit having a general purpose input/output (GPIO) line;

 a first circuit component coupled to the GPIO line, wherein the first circuit

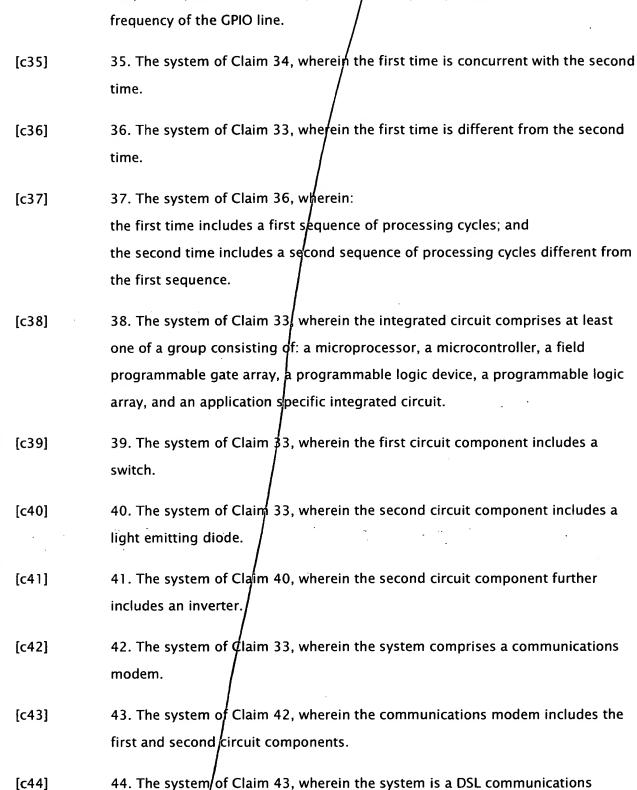
 component is adapted to provide, at a first time, a first input to the integrated

 circuit using the GPIO line; and

 a second circuit component coupled to the GPIO line, wherein the second circuit

 component is adapted to receive, at a second time, a first output from the

 integrated circuit using the GPIO line.
- [c34] 34. The system of Claim 33, wherein the first circuit component further is



adapted to provide the first input at a low frequency relative to a switching

system.